

<p>2. Compositing motion graphic: Images depicting 21st century high tech: computers, smart phones, similar. Add historical images: Wright Brothers' first flight, first telephone. Change visuals to images depicting globally connected world: Internet, GPS, video, etc.</p>	<p><u>Fade in new music theme</u></p> <p>(2) <u>NARRATOR</u> (VO): Did you ever think we'd be here – in a world where technology thinks and moves faster than the human brain?</p> <p>After all, it wasn't that long ago that the Wright Brothers took to the air and Alexander Graham Bell made the first phone call.</p> <p>Today our globally-connected world is a direct result of this heritage of technological innovation.</p>
<p>3. Venn diagram: see brochure pg. 2. Animate three circles together.</p> <p>Add SmartFusion logo in the middle.</p> <p>Label each circle in order: FPGA ARM Cortex-M3 Programmable Analog</p>	<p>(3) As innovation pushes forward, integration is the key that makes our digital lives smarter and faster.</p> <p>Welcome to the world of SmartFusion, the integration of</p> <p>a full featured FPGA, an ARM Cortex M3 processor, and programmable analog in a single device.</p>

<p>4. SmartFusion Architecture block diagram, see brochure page 3. Highlight ProASIC FPGA architecture (purple).</p> <p>Add text as mentioned:</p> <ul style="list-style-type: none"> • ProASIC FPGA • 130nm, CMOS • Densities from 60-500K system gates • 350 MHZ performance, up to 2020 I/Os. 	<p>(4) SmartFusion is a fully programmable design platform for complex embedded designs.</p> <p>SmartFusion devices feature Actel’s proven, flash-based ProASIC3 FPGA architecture.</p> <p>Built on an advanced 130 nano-meter, CMOS process, Actel offers densities ranging from 60 K to 500 K system gates, with 350 MHZ performance and up to 204 I/Os.</p> <p>This combination of density and I/O count allows for integration of existing functions from other devices. This substantially reduces board size, complexity, and power consumption of the overall system.</p>
<p>5. SmartFusion Architecture block diagram, see brochure page 3.</p> <p>Now highlight ARM Cortex M-3 section (blue).</p> <p>List out peripherals as mentioned:</p> <ul style="list-style-type: none"> • Multi-layer AHB matrix with up to 16 Gbps throughput • 10/100 Ethernet MAC with RMIi interface 	<p>(5) Intelligence is added to the FPGA in the form of the microcontroller subsystem which features a hard ARM Cortex-M3 running at 100MHz. A full complement of processor peripherals include:</p> <ul style="list-style-type: none"> • Multi-layer AHB communications matrix with up to 16 Gbps throughput, • 10/100 Ethernet MAC with RMIi interface,

<p>5 CONT.</p> <ul style="list-style-type: none"> • Two each: SPI, I2C, UART, 32-bit Timers • Up to 512 KB flash and 64KB SRAM • External Memory Controller • 8-channel DMA. 	<ul style="list-style-type: none"> • Two of each: SPI, I2C, UART, 32-bit timers, • Up to 512 KBytes of nonvolatile flash memory and 64 KBytes of SRAM, • Multi-layer AHB communications matrix with up to 16 Gbps throughput, • External memory controller, and • 8-channel DMA controller.
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<p>6. SmartFusion Architecture block diagram, see brochure page 3. Now highlight Analog area (yellow). Highlight ACE section. Add text: ACE. Add text bullets as mentioned:</p> <ul style="list-style-type: none"> • ADCs and DACs with 1% accuracy • Up to 3 12-bit ADCs with up to 600Kbps sampling rate • Up to 3 12-Bit first order Sigma Delta DACs • Up to 10 50 ns high-speed comparators • Multiple integrated temperature, voltage, current monitors 	<p>(6) The innovative and proprietary analog compute engine - ACE - performs sample sequencing and processing, which offloads the Cortex-M3 processor from analog initialization and processing. The programmable analog system features:</p> <ul style="list-style-type: none"> • ADCs and DACs with 1 percent accuracy, • Up to three 12-Bit ADCs with up to 600 Kbps sampling rate, • Up to three 12-Bit first order sigma delta DACs • Up to ten 50 ns high-speed comparators, • Multiple integrated temperature, voltage and current monitors.
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<p>7. Venn diagram animation, SmartFusion logo in middle, Add text to each circle as mentioned:</p> <ul style="list-style-type: none"> • Full Design Customization • Ease-of-Use <p>(Maybe the Venn diagram could be next to or in front of visuals that depict each of the areas as mentioned.)</p>	<p>(7) SmartFusion's unprecedented integration provides:</p> <ul style="list-style-type: none"> • Full design customization to optimize hardware / software tradeoffs on the fly without board level changes, and remarkable Ease-of-use. <p>Actel's Libero IDE and SoftConsole deliver easy and natural design flows for both FPGA and embedded designers.</p>
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<p>7A. Continue Venn Diagram graphic by labeling third circle “IP Protection”</p> <p>Transition to:</p> <p>SmartFusion chip icon or image.</p> <p>Add animated arrows depicting secure data flow.</p> <p>Transition to:</p> <p>CU of logic unit area on SmartFusion. Add text: “Nonvolatile”</p> <p>Add text or icon/logo: FlashLock</p>	<p>(7A) Intellectual property protection is superior to any other integrated or discrete solution in the market.</p> <p>In SmartFusion, all the data transferred from the processor to the FPGA, or from the analog to the processor, or between the FPGA and the analog, are on-chip and secure.</p> <p>Additionally, every logic cell in our flash FPGA is non-volatile and thus does not require the use of an external configuration device. Because there’s no bit-stream transfer to intercept, your IP is protected against theft.</p> <p>Actel FPGAs feature FlashLock, a 128 bit hardware key that controls access to the device’s security settings. The key can be used to reopen the security setting later.</p>
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<p>9. Graphic: Build on three icons or images depicting the three types of designers: FPGA, Embedded, Analog.</p> <p>Add insert boxes with screen grabs of various software tools as mentioned. Other ideas?</p>	<p>(9) Whether you're an FPGA designer with a desire to offload communication management and sequencing functions, or an embedded designer with a need for hardware algorithm acceleration, or a designer wanting to enhance analog usage and integration, SmartFusion offers the ideal design platform for design teams or individuals.</p> <p>For FPGA Designers, Actel offers Libero IDE: a comprehensive design environment for designing all Actel FPGAs.</p> <p>For Embedded Designers, Actel offers support through SoftConsole , Keil, or IAR.</p> <p>The MSS Configurator creates a bridge between the FPGA and embedded design, so device configuration can be easily shared between multiple developers.</p> <p>And for Analog Design, the MSS Configurator provides graphical setup of current, voltage, and temperature monitors, sample sequencing set-up, and post processing configuration, as well as configuration of the DAC outputs.</p>
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<p>10. Graphic: SmartFusion Head with animation, Build on text bullets as mentioned:</p> <ul style="list-style-type: none"> • Low Power • IP Security • SEU Immunity and Reliability 	<p>(10) Remember that only Actel’s flash technology allows for the integration of an FPGA, a complete microcontroller subsystem with a hard ARM cortex-M3 and programmable analog On a single chip.</p> <p>Don’t expect to see this from any other FPGA vendor.</p>
<p>11. Opening graphics animation background, fly through text as mentioned:</p> <p>Innovative,</p> <p>Intelligent</p> <p>Integration</p> <p>Fly through “head graphic”</p> <p>Fly in and hold on Actel logo</p> <p>FADE OUT with music</p>	<p>(11) Innovative</p> <p>Intelligent</p> <p>Integration.</p> <p>Get Smart</p> <p>with SmartFusion,</p> <p>only from Actel.</p> <p><u>Music pays off and fade out</u></p>